EO 901 653 365 US

TITLE

DEVICE AND METHOD FOR DETECTING ALIGNMENT OF ACTIVE AREAS AND MEMORY CELL STRUCTURES IN DRAM DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to test devices, and more particularly, to a test device for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors, as well as a test method thereof.

Description of the Related Art

With the wide application of integrated circuits (ICs), several kinds of semiconductor devices with higher efficiency and lower cost are presently produced based on different objectives, making DRAM an important semiconductor device in the information and electronics industry.

Most DRAM carries one transistor and one capacitor in a single DRAM cell. The memory capacity of the DRAM can reach 256MB. Therefore, with increased integration it is necessary to reduce the size of memory cells and transistors to accommodate DRAM with higher memory capacity and processing speed. A 3-D capacitor structure can reduce the occupied area on the semiconductor substrate, such as with a deep trench capacitor, and is applicable to the fabrication of the DRAM with capacity of 64MB and above.

As compared with a traditional plane transistor, however, this structure covers many areas of the semiconductor substrate and cannot satisfy the demands of high integration.

Therefore, a vertical transistor which can save space is important in structuring a memory unit.

The adjacent memory cells may experience current leakage and cell failure, reducing process yield, if active area masks and memory cell structures are not aligned accurately. Therefore, process yield and reliability of the memory cells can be improved if alignment accuracy between the masks of active areas and memory cell structures is controlled within an acceptable range.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to detect alignment of active areas and memory cell structures in DRAM devices with vertical transistors.

According to the above mentioned object, the present invention provides a test device and method for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors.

In the test device of the present invention, parallel first and second memory cell structures disposed in the scribe line region, each has a deep trench capacitor and a transistor structure. An active area is disposed between the first memory and second memory cell structures. The active area overlaps the first and second memory cell structures by a predetermined width. First and second conductive pads are disposed on both ends of the first memory cell structure respectively, and third and fourth conductive pads are disposed on both ends of the first memory cell structures respectively.

According to the present invention, a method for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors includes the following steps. First, a wafer with at least one scribe line region and at least one memory region is provided. Then, a plurality of memory cells in the memory region and at least one test device in the scribe line region are formed simultaneously. A first resistance between the first and second conductive pads disposed on the first memory cell structure is measured. A second resistance between the third and fourth conductive pads disposed on the second memory cell structure is measured. Next, alignment of the active area and the first and second memory cell structures is determined according to the first resistance and the second resistance. Finally, alignment of the active area and the memory cells in the memory region is determined according to alignment of the active area and the first and second memory cell structures of the test device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Fig. 1 is a cross section of a memory device with vertical transistors;

Fig. 2 is a layout of the memory device as shown in Fig. 1;

Fig. 3 is a layout of the test device according to the present invention; and

Fig. 4 is another layout of the test device with alignment shift according to the present invention;

Fig. 5 is a cross section of the test device according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the present invention, at least one test device 200 is formed in the scribe line region, while a plurality of memory cells with vertical transistors is formed in the memory regions on a wafer simultaneously. The plurality of memory cells formed in the memory region is shown in Fig. 1 and Fig. 2 and the test device 200 is shown in Fig. 3.

As shown in Fig. 1, deep trench capacitors 102 are formed into a matrix and disposed in the substrate 100. Each deep trench capacitor 102 has a vertical transistor 104 disposed thereon. Each vertical transistor 104 includes a gate 104a, a gate oxide layer 104b, a source 104c and a common drain 104d. The gate oxide layer 104b is the sidewall at the bottom of the gate 104a, and the vertical region between the source 104c and the common drain 104d in the substrate 100 is the channel of the transistor 104.

As shown in Fig. 2, word lines 118a, 118b, 118c and 118d are disposed above the active area 112 as the gate 104a of the transistor 104 (not shown). Command drains 104d are disposed above the active areas 112 between adjacent word lines 118a and 118b or 118c and 118d. Bit lines 116a and 116b are perpendicular to word lines 118a~118d, and are electrically coupled to the command drains through bit line contacts 114.

Fig. 3 is a layout of the test device of the present invention. The test device 200 detects the alignment of active areas and memory cell structures in DRAM devices with vertical transistors, wherein the test device 200 is disposed in a scribe line region of a wafer (not shown).

In test device 200 shown in Fig. 3, parallel first and second memory cell structures TC_1 and TC_2 are disposed in the scribe line region (not shown), each has a deep trench capacitor and a transistor structure. An active area A_1 is disposed between the first memory cell structure TC_1 and the second memory cell structures TC_2. The active area A_1 overlaps the first and second memory cell structures (TC_1 and TC_2) a predetermined overlap width W. First and second conductive pads (GC_1 and GC_2) are disposed on both ends of the first memory cell structures TC_1 respectively, and third and fourth conductive pads (GC_3 and GC_4) are disposed on both ends of the first memory cell structures TC_2 respectively.

In the present invention, two parallel deep trenches in the scribe line region and a plurality of deep trenches in the memory region are formed simultaneously. Then, the parallel first and second memory cell structures TC_1 and TC_2 are formed in the two parallel deep trenches and the memory cells with vertical transistors are formed in the deep trenches in the memory region simultaneously. The parallel first and second memory cell structures TC_1 and TC_2, each has a deep trench capacitor and a transistor structure.

Next, active areas 112 in the memory region and an active area A_1 in the scribe line region are formed simultaneously with the same process and conditions. The active area A_1 is formed between the memory cell structures TC_1 and TC_2, and

overlaps the memory cell structures TC_1 and TC_2 by a predetermined overlap width W respectively.

The word lines 118a~118b of the memory cells in the memory regions and the first to fourth conductive pads GC_1~GC_4 on the memory cell structures TC_1 and TC_2 are formed simultaneously with the same masks, process and conditions. The first and second conductive pads GC_1 and GC_2 are disposed on both ends of the first memory cell structure TC_1 respectively. The third and fourth conductive pads GC_3 and GC_4 are disposed on both ends of the second memory cell structure TC_2 respectively. The first to fourth conductive pads and the bar-type conductive pad are made of the same material, such as polysilicon. The first and second conductive pads GC_1 and GC_2 are electrically coupled to the transistor structure (gate) under the deep trench capacitor of the first memory cell structure TC_1 respectively. The third and fourth conductive pads GC_3 and GC_4 are electrically coupled to the transistor structure (gate) under the deep trench capacitor of the second memory cell structures TC_2 respectively. In addition, the first conductive pad GC_1 are a predetermined distance L from the second conductive pad GC_2, and the third conductive pad GC_1 are the predetermined distance L from the fourth conductive pad GC_4.

With reference to Fig. 4 and Fig. 5, normally, a first resistance R_1 between the first conductive pad GC_1 and the second conductive pad GC_2 on both ends of the first memory cell structure TC_1 can be detected. A second resistance R_2 between the third conductive pad GC_3 and the fourth conductive pad GC_4 on both ends of the second memory cell structure TC_2 can be

detected. The first resistance R_1 and the second resistance R_2 can be obtained according to equations 1 and 2.

$$R_1 = R_{CT} \times \frac{L}{W + \Delta W}; \quad (1)$$

$$R_2 = R_{CT} \times \frac{L}{W - \Delta W}; \quad (2)$$

Wherein R_{CT} is the resistance per surface area of memory cell structures (TC_1 and TC_2), L is the predetermined distance between the first and second conductive pads (GC_1 and GC_2) and between the third and fourth conductive pads (GC_3 and GC_4) respectively, $W+\Delta W$ is the overlap width between the active area A_1 and the first memory cell structure TC_1, and $W-\Delta W$ is the overlap width between the active area A_1 and the second memory cell structure TC_2. Using the same process, material and conditions, equations 3 and 4 can be achieved according to the equations 1 and 2.

$$\frac{R_1}{R_2} = \frac{W - \Delta W}{W + \Delta W}; \quad (3)$$

$$\Delta W = W \times \frac{R_2 - R_1}{R_2 + R_1}; \quad (4)$$

Thus, the alignment shift ΔW between the active area A_1 and the first and second memory cell structure TC_1 and TC_2 can be obtained if the first resistance R_1 and the second resistance R_2 are measured. That is to say, the alignment shift ΔW of the active area A_1 and the first and second memory cell structures (TC_1 and TC_2) is zero when the first resistance R_1 equals the second resistance R_2.

With reference to Fig. 4 and Fig. 5, the active area A_1 is shifted by a distance ΔW along the direction DIR_1 if the masks of the first and second memory cell structure (TC_1 and

TC_2) and the active area A_1 have an alignment shift ΔW in the direction DIR_1. If this condition is met, the first resistance R_1 is smaller than the second resistance R_2 according to the equations 1 and 2. Moreover, the alignment shift ΔW can be obtained according to the equation 4.

On the contrary, the active area A_1 is shifted by a distance ΔW along the direction DIR_2 if the masks of the first and second memory cell structures (TC_1 and TC_2) and the active area A_1 have an alignment shift ΔW in the direction DIR_2. If this condition is met, the first resistance R_1 is larger than the second resistance R_2 according to the equations 1 and 2. Moreover, the alignment shift can be obtained according to the equation 4.

In the present invention, the test device 200 disposed in the scribe line region and a plurality of memory cells with vertical transistors in the memory region are formed simultaneously. For example, the deep trench capacitor and transistor structure of the memory cells in the memory region and the deep trench capacitor and transistor structure of the memory cell structures (TC_1 and TC_2) in the scribe line region are formed simultaneously with the same masks, process and conditions. The active areas 112 of the memory cells in the memory region and the active area A_1 of the test device 200 are formed simultaneously with the same masks, process and conditions. Therefore, the memory region and the test device may have the same alignment shift between memory cell structures (TC_1 and TC_2) and active areas (112 and A_1) use of the same masks and the same process. Thus, alignment of memory cell structures and active areas in the memory region can be

obtained according to whether the first resistance R_1 equals the second resistance R_2.

The present invention also provides a method for detecting alignment of memory cell structures and active areas in memory devices with vertical transistors. In the method of the present invention, a wafer with at least one scribe line region and at least one memory region is provided.

A plurality of memory cells with vertical transistors in the memory region and at least one test device in the scribe line region are formed simultaneously, wherein each memory cell has a deep trench capacitor and a corresponding transistor structure (memory cell structure) as shown in Fig. 1 and Fig. 2. The structure of the test device 200 is shown in Fig. 3. The memory cell structure in the memory regions and the memory cell structure (TC_1 and TC_2) in the test device 200 are formed by the same mask and the same process. The active areas 112 in the memory regions and the active area A_1 in the test device 200 are formed with the same mask and process.

Next, a first resistance R_1 between the first conductive pad GC_1 and the second conductive pad GC_2 on both ends of the first memory cell structure TC_1 is determined. A second resistance R_2 between the third conductive pad GC_3 and the fourth conductive pad GC_4 on both ends of the second memory cell structure TC_2 is determined. Then, alignment of the active area A_1 and the first and second memory cell structures TC_1 and TC_2 of the test device 200 is determined according to whether the first resistance R_1 is equal to the second resistance R_2.

The memory region and the test device may have the same alignment shift between active areas (A_1 and 112) and memory cell structures (TC_1 and TC_2) use the same masks and the same process. Thus, alignment of active areas and memory cell structures in the memory region can be obtained according to whether the first resistance R_1 equals the second resistance R_2. The alignment shift between active areas and memory cell structures in the memory regions can also be obtained according to the equation 4.

Further, in the present invention the test device is disposed in the scribe line region to avoid occupying layout space.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.